Haopeng Zeng

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Education

University of Southern California **Jan. 2024 – Dec. 2025**
Master of Science in Electrical Engineering (GPA: 3.75) *Los Angeles, CA*

University of California, Santa Cruz **Sep. 2018 – June 2022**
Bachelor of Science in Computer Science (GPA: 3.74) *Santa Cruz, CA*

Relevant Coursework

- Complex Digital ASIC System Design
- Computer System Organization
- MOS VLSI Circuit Design
- Digital Systems Design
- Computer Systems Architecture (In Progress)
- Network Processor Design and Programming (In Progress)

Experience

University of Southern California - iLab **Jan. 2024 – Present**
Research Assistant *Los Angeles, CA*

- Create Python and Bash scripts to automate ROS workflows and partition ROS bag data for downstream 3D reconstruction tasks.
- Implement the motion model for a navigation robot by incorporating differential drive systems and conducting 6D pose estimations. Establish a reinforcement learning environment to train ML models using OpenAI's Gymnasium.

Projects

Intel 16nm CNN Accelerator ASIC | *Tape-out Project, SystemVerilog* **Dec. 2024**

- Contributed in all steps from RTL to GDSII design flow, leading to a successful tape-out on Intel's 16nm technology.
- Implemented an Eyeriss V1-based architecture featuring energy-efficient row-stationary data flow, reducing data movement and power consumption while supporting convolution, max pooling, and ReLU.
- Led RTL design and verification within a 4-person team; employed direct and randomized testing methodologies for comprehensive verification and automated test flows using Python scripts.
- Achieved a maximum clock frequency of 1GHz.
- Used Cadence and Synopsys EDA tools for synthesis, P&R, DRC, and LVS.

Tomasulo 32-bit Out-of-Order Execution CPU | *VHDL, ModelSim* **June 2024**

- Developed key features including branch prediction, speculative execution, and memory disambiguation.
- Implemented modules such as the Issue Unit, Re-order Buffer (ROB), Free Register List (FRL), Store Buffer, Store Address Buffer, and a 2-stage Dispatch Unit.
- Developed a copy-free checkpoint (CFC) technique optimized for FPGA, enabling efficient restoration of the Front-End Register Alias Table (FRAT) during branch misprediction events.

Advanced eXtensible Interface (AXI) Interconnect | *Verilog, ModelSim* **June 2024**

- Developed AXI protocol bridging interface in Verilog that packetized read/write transactions for a multi-master, multi-slave SoC.
- Utilized reorder buffers to maintain in-order transactions for each master's writes and reads, while supporting out-of-order behavior across different masters and memories.

PCIe (Physical Layer) Implementation | *Verilog, ModelSim* **July 2024**

- Implemented 8b/10b encoding for PCIe interfaces, enhancing data integrity and stability by ensuring DC balance
- Completed Elastic Buffer to handle transmissions across different clock domains
- Developed De-Skew FIFO to eliminate lane-to-lane skew, ensuring synchronization across multiple lanes.

Technical Skills

Languages: SystemVerilog, Verilog, VHDL, C/C++, Python, JavaScript
Tools/Technologies: Cadence Virtuoso, Genus, Innovus, Synopsys VCS, Xilinx Vivado, ModelSim, FPGA, Linux, Git